First in-beam commissioning test of AIDA

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This The Advanced Implantation Detector Array (AIDA) [1] is a state of the art detector system designed for the study of the radioactive decay of exotic nuclei at the SuperFRS, FAIR and other applications, for example, reaction studies with radioactive ion beams. AIDA has been designed and developed by a collaboration between the University of Edinburgh (the lead research organisation), the University of Liverpool and the STFC Daresbury and Rutherford Appleton Laboratories. High-energy, exotic nuclei will be implanted into a multi-plane double-sided silicon strip detector (DSSSD) system. Subsequent correlated radioactive decays are detected by the DSSSDs and surrounding neutron and gamma-ray detector systems. To instrument the DSSSDs a 16-channel application specific integrated circuit (ASIC) has been developed. The ASIC provides asynchronous readout, selectable gain (20MeV or 1GeV FSR) and a novel overload recovery circuit providing high energy (20GeV FSR) operation and sensitivity to fast, low-energy decays. To provide a fully integrated ASIC control and data acquisition system a front end electronics (FEE) module has been produced which incorporates readout of four ASICs (64 channels) via an analogue multiplexor (MUX) and 1MHz, 16-bit and 50MSPS 14-bit sampling ADCs using a Xilinx Virtex 5 FPGA incorporating a PowerPC 604 CPU running Linux and Gbit ethernet interface.

A system consisting of an MSL Type W(DS)-1000 DSSSD and prototype AIDA FEE and ASIC hardware was tested with beta-delayed protons from ^{33}Ar ions produced by 40MeV/u ^{36}Ar incident on a cryogenic, 2 bar H_2 target and selected by MARS. This enabled the prototype AIDA hardware to be tested with high energy ions for the first time. A range of systematic tests were performed and implant-decay event correlation using an internal clock was demonstrated. It should be emphasised that it is difficult to reproduce such tests in bench tests or computer simulations due to the complexity of the DSSSD, ac coupling, bias network and ASIC input interactions, and that these tests therefore provided unique information. As a direct consequence of these tests, significant design revisions of the AIDA ASIC input stage, FEE power distribution and regulation network, and FPGA VHDL hardware have been undertaken. Production runs of the AIDA ASIC and FEE hardware are now reaching completion and we expect commissioning tests of the production hardware to be performed in the second half of 2011.

[1] D. Braga *et al.*, AIDA: *A 16-channel amplifier ASIC to read out the advanced implantation detector array for experiments in nuclear decay spectroscopy*, IEEE NSS 2009 IEEE pp.1924; doi:10.1109/NSSMIC.2009.5402153